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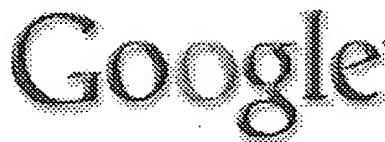
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... Publications. Brian Beckman. Beckman, BR and WT Peterson. 1986. ... 44:14-17.

Dickhoff, WW, BR Beckman, DA Larsen, C. Duan, and S. Moriyama. 1997. ...

[www.nwfsc.noaa.gov/research/staff/display\\_publications.cfm?staffid=412&staffprofileid=280&name=Br...](http://www.nwfsc.noaa.gov/research/staff/display_publications.cfm?staffid=412&staffprofileid=280&name=Br...) - 22k - Mar 9, 2004 - [Cached](#) - [Similar pages](#)
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Brian C Merrell: "Re: Linux Expo Tent Event..."; Reply: Brian C Merrell ...

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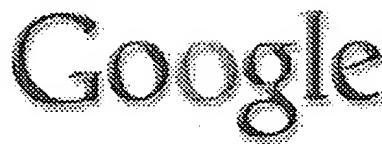
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### Lookahead revisited in wireless network simulations

... Authors, **Jason** Liu, Dartmouth College, Hanover, NH. ... 1 L. Ahlin and J. **Zander**. Principles of wireless communications, 2nd Edition. ...  
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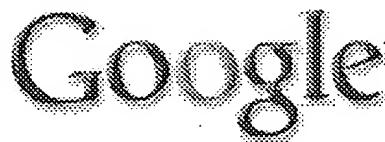
   
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**1** An efficient profile-analysis framework for data-layout optimizations 100%  
 Shai Rubin , Rastislav Bodík , Trishul Chilimbi  
**ACM SIGPLAN Notices , Proceedings of the 29th ACM SIGPLAN-SIGACT symposium on Principles of programming languages** January 2002  
Volume 37 Issue 1  
Data-layout optimizations rearrange fields within objects, objects within objects, and objects within the heap, with the goal of increasing spatial locality. While the importance of data-layout optimizations has been growing, their deployment has been limited, partly because they lack a unifying framework. We propose a parameterizable framework for data-layout optimization of general-purpose applications. Acknowledging that finding an optimal layout is not only NP-hard, but also poorly approxima ...

**2** Memory forwarding: enabling aggressive layout optimizations by 89%  
 guaranteeing the safety of data relocation  
Chi-Keung Luk , Todd C. Mowry  
**ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture** May 1999  
Volume 27 Issue 2  
By optimizing data layout at run-time, we can potentially enhance the performance of caches by actively creating spatial locality, facilitating prefetching, and avoiding cache conflicts and false sharing. Unfortunately, it is extremely difficult to guarantee that such optimizations are *safe* in practice on today's machines, since accurately updating *all* pointers to an object requires perfect alias information, which is well beyond the scope of the compiler for languages such as C. T ...

**3** Improving locality using loop and data transformations in an integrated 87%  
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... To address this, we propose a **data layout optimization** framework that replaces the current profile-directed approach with an iterative profile-feedback approach ...

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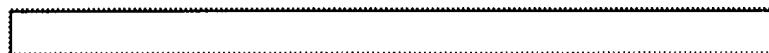
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**1** Using generational garbage collection to implement cache-conscious 77%

 data placement

Trishul M. Chilimbi, James R. Larus

**ACM SIGPLAN Notices, Proceedings of the first international symposium on  
Memory management** October 1998

Volume 34 Issue 3

The cost of accessing main memory is increasing. Machine designers have tried to mitigate the consequences of the processor and memory technology trends underlying this increasing gap with a variety of techniques to reduce or tolerate memory latency. These techniques, unfortunately, are only occasionally successful for pointer-manipulating programs. Recent research has demonstrated the value of a complementary approach, in which pointer-based data structures are reorganized to improve cache loca ...

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Erez Petrank , Dror Rawitz

**ACM SIGPLAN Notices , Proceedings of the 29th ACM SIGPLAN-SIGACT symposium on Principles of programming languages** January 2002

Volume 37 Issue 1

The growing gap between the speed of memory access and cache access has made cache misses an influential factor in program efficiency. Much effort has been spent recently on reducing the number of cache misses during program run. This effort includes wise rearranging of program code, cache-conscious data placement, and algorithmic modifications that improve the program cache behavior. In this work we investigate the complexity of finding the optimal placement of objects (or code) in the memory, ...

**2** Cache-conscious data placement 80%

Brad Calder , Chandra Krintz , Simmi John , Todd Austin

**Proceedings of the eighth international conference on Architectural support for programming languages and operating systems** October 1998

Volume 33 , 32 Issue 11 , 5

As the gap between memory and processor speeds continues to widen, cache efficiency is an increasingly important component of processor performance. Compiler techniques have been used to improve instruction cache performance by mapping code with temporal locality to different cache blocks in the virtual address space eliminating cache conflicts. These code placement techniques can be applied directly to the problem of placing data for improved data cache performance. In this paper we present a gene ...

**3** Using generational garbage collection to implement cache-conscious data placement 77%

Trishul M. Chilimbi , James R. Larus

**ACM SIGPLAN Notices , Proceedings of the first international symposium on Memory management** October 1998



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**1** Cache-conscious structure layout 97%  
 Trishul M. Chilimbi , Mark D. Hill , James R. Larus  
**ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1999 conference on Programming language design and implementation** May 1999  
 Volume 34 Issue 5

Hardware trends have produced an increasing disparity between processor speeds and memory access times. While a variety of techniques for tolerating or reducing memory latency have been proposed, these are rarely successful for pointer-manipulating programs. This paper explores a complementary approach that attacks the source (poor reference locality) of the problem rather than its manifestation (memory latency). It demonstrates that careful data organization and layout provides an essential mech ...

**2** Cache-conscious data placement 96%  
 Brad Calder , Chandra Krintz , Simmi John , Todd Austin  
**Proceedings of the eighth international conference on Architectural support for programming languages and operating systems** October 1998  
 Volume 33 , 32 Issue 11 , 5

As the gap between memory and processor speeds continues to widen, cache efficiency is an increasingly important component of processor performance. Compiler techniques have been used to improve instruction cache performance by mapping code with temporal locality to different cache blocks in the virtual address space eliminating cache conflicts. These code placement techniques can be applied directly to the problem of placing data for improved data cache performance. In this paper we present a gene ...

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